Reg.No. ____________

Karunya UNIVERSITY

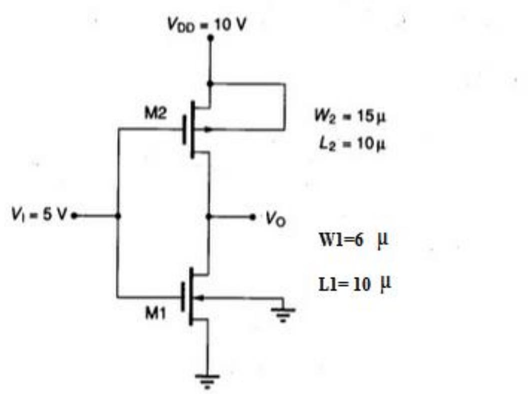
(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – Nov/Dec – 2016

			Semester :	**2016-17 ODD**
Code :	**14EC3056**		**Duration :**	**3hrs**
Sub. Name :	**Analog VLSI Design**		**Max. marks :**	**100**

ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)

Q. No.	Sub Div.	Questions	Course Outcome	Marks
1.	a.	Explain in detail about dc BJT model and also discuss the forward and reverse active regions of operation.	CO1	**12**
	b.	Obtain the non zero small signal model parameter for MOSFET model.	CO1	**8**
		(OR)		
2.	a.	Calculate all of the parasitic capacitors for M1 in the following circuit. Use the CMOS process parameters of Table 2B.49(attached below).Assume the area of the sources of both M1 and M2 are 90μ^2 and that the drain areas of M1 and M2 are each 50 μ^2.Neglect junction side wall capacitance. 	CO1	**10**
	b.	Differentiate Sah's and Shichman-Hodges model and obtain the equivalent circuits for MOSFET in ohmic and saturation region.	CO1	**10**
3.	a.	Explain in detail about High frequency BJT Model.	CO1	**8**
	b.	With block diagram explain about D/A converter and also illustrate about dynamic performance of the same.	CO3	**8**
	c.	The input of a 3-bit DAC is $(101)_2$ & V_{ref}=5V. Find fraction of output voltage (F),V_{FS}, and LSB.	CO3	**4**
		(OR)		
4.	a.	Discuss the voltage scaling technique in DAC in detail.	CO3	**8**
	b.	Find the output voltage for binary bit '100' using R-2R ladder method. Assume V_{ref} = 3V.	CO3	**5**

	c.	Discuss the current scaling technique in D/A converters with neat diagrams.	CO3	**7**
5.	a.	With neat block diagram explain about self calibrating A/D Converter.	CO3	**10**
	b.	If C1=C2=C, find the value of C that will emulate a 1MΩ resistor if the clock frequency is 250kHz.	CO2	**3**
	c.	Design a parallel switched capacitor realization of a resistor.	CO2	**7**
		(OR)		
6.	a.	List out the properties of Butter worth filter, Chebyshev filter, Elliptic filter and Bessel filter and explain in detail about Low pass filter.	CO3	**10**
	b.	Explain in detail about Parallel A/D Converters.	CO3	**10**
7.	a.	Explain the characteristics of differential amplifier and explain the condition to make the transistor to work in saturation region for differential amplifier with current mirror as active load.	CO3	**10**
	b.	Explain in detail about High speed comparator.	CO3	**10**
		(OR)		
8.	a.	Explain in detail about different types of open loop comparators.	CO3	**15**
	b.	Draw the circuit diagram of differential amplifier with current source as active load.	CO3	**5**
		Compulsory:		
9.	a.	Design high gain amplifier with suitable expressions.	CO3	**10**
	b.	Explain in detail about data conversion process in SAR ADC.	CO3	**10**

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TABLE 2B.4

Process parameters for a typical[a] p-well CMOS process

	Typical	Tolerance[b]	Units
Square law model parameters			
V_{T0} (threshold voltage)			
n-channel (V_{TN0})	0.75	± 0.25	V
p-channel (V_{TP0})	−0.75	± 0.25	V
K' (conduction factor)			
n-channel	24	± 6	$\mu A/V^2$
p-channel	8	± 1.5	$\mu A/V^2$
γ (body effect)			
n-channel	0.8	± 0.4	$V^{1/2}$
p-channel	0.4	± 0.2	$V^{1/2}$
λ (channel length modulation)			
n-channel	0.01	± 50%	V^{-1}
p-channel	0.02	± 50%	V^{-1}
ϕ (surface potential)			
n- and p-channel	0.6	± 0.1	V
Process parameters			
μ (channel mobility)			
n-channel	710		$cm^2/(V \cdot s)$
p-channel	230		$cm^2/(V \cdot s)$
Doping[c]			
n^+ active	5	±4	$10^{18}/cm^3$
p^+ active	5	±4	$10^{17}/cm^3$
p-well	5	±2	$10^{16}/cm^3$
n-substrate	1	±0.1	$10^{16}/cm^3$
Physical feature sizes			
T_{OX} (gate oxide thickness)	500	± 100	Å
Total lateral diffusion			
n-channel	0.45	± 0.15	μ
p-channel	0.6	± 0.3	μ
Diffusion depth			
n^+ diffusion	0.45	± 0.15	μ
p^+ diffusion	0.6	± 0.3	μ
p-well	3.0	± 30%	μ
Insulating layer separation			
POLY I to POLY II	800	± 100	Å
Metal 1 to Substrate	1.55	± 0.15	μ
Metal 1 to Diffusion	0.925	± 0.25	μ
POLY I to Substrate (POLY I on field oxide)	0.75	± 0.1	μ
Metal 1 to POLY I	0.87	± 0.7	μ
Metal 2 to Substrate	2.7	± 0.25	μ
Metal 2 to Metal I	1.2	± 0.1	μ
Metal 2 to POLY I	2.0	± 0.07	μ

Note: $K' = \mu C_{ox}$ 24E-6 ≠ (710)(.07) ≈ 49.7E-6